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10/563,995	01/09/2006	Andrea Milanesi	DE03 0240 US1	7025

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EXAMINER	
MORRIS, JOHN J	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/563,995	MILANESI, ANDREA	
	Examiner	Art Unit	
	John Morris	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-10, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat# 4555673/ *or "Huijsing" hereinafter*) in view of Schade, JR. (US Pat# 4392112/ *or "Schade" hereinafter*).

For **claim 1,** Huijsing teaches an apparatus comprising an input stage with an NMOS transistor doublet having a first differential input for receiving input signals and a PMOS transistor doublet having a second differential input for receiving input signals (Huijsing, figure 2). Huijsing also teaches constant transconductance (Huijsing, abstract). Huijsing does not teach a switching means; however, in the same field of endeavor, Schade teaches an amplifier with switching means for receiving and selectively directing analog input signals only to one of either said first differential input or to said second differential input (Schade, figure 1). Schade also teaches a switching signal and for

connecting the other one of the first and second differential inputs to a reference voltage responsive to switching signal (Schade, column 3, lines 1 - 33).). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Huijsing with Schade because both deal with the amplifiers and the addition of the switches would reduce power consumption.

For **claim 2,** Huijsing teaches controlling the current to control the transconductance (Huijsing, abstract). Huijsing does not teach switching means; however, in the same field of endeavor, Schade teaches a plurality of switches direct the analog input signals to said first differential input and to second differential input (Schade, figure 1). Therefore, it would have been obvious to control the switches in a way to control the transconductance such that input signals to the first differential input if the signals have positive gamma data and to second differential input if the input signals have negative gamma data.

For **claim 3,** Huijsing teaches the NMOS transistor doublet comprises two NMOS transistors, each having a gate, whereby the gate of the first of the two NMOS transistors is connectable to a first input node and the gate of the second of the two NMOS transistors is connectable to a second input node, the PMOS transistor doublet comprises two PMOS transistors, each having a gate, whereby the gate of the first of the two PMOS transistors is connectable to the first input node and the gate of the second of the two PMOS transistors is connectable to the second input node (Huijsing, figure 1 and 2).

Huijsing does not teach switching means; however, in the same field of endeavor, Schade teaches a plurality of switches connected to the transistor doublets (Schade, figure 1).

For **claim 5**, Huijsing teaches a rail-to-rail input stage (Huijsing, abstract).

For **claim 6,** Schade teaches an amplifier circuit with a plurality of switches to selectively direct the input signals wherein the NMOS doublet active when the analog input signals are directed to the second differential input and to keep the PMOS transistor doublet active when the analog input signals are directed to the first differential input switching means comprise a plurality of switches in order to selectively direct the input signals to said first differential input or said second differential input (Schade, figure 1, items S1 to S6).

For **claim 7,** Huijsing and Schade do not teach a digital switch; however, the examiner takes official notice that it would have been an obvious matter of design choice to use a digital signal to control the switching circuit since the signal only needs to have two states, on and off.

For **claim 8**, Schade teaches that the switches can be transistors (Schade, column 3, lines 1 - 33).

For **claim 9,** Huijsing teaches transistor doublets as part of a folded cascade rail-to-rail input stage and wherein the folded cascade rail-to-rail input stage is connected to a second stage comprising a rail-to-rail output stage amplifier (Huijsing, figure 1 and 3b).

For **claim 10,** Huijsing and Schade do not teach a source driver bank; however, the examiner takes official notice that this would have obvious to one of ordinary skill in the art to have a plurality of apparatus' in a driver bank since such a modification would only require a mere replication of the apparatus. It is also well known that a bus is used for receiving input signals since a bus may only be an electrical connection use to transfer data.

For **claim 12,** Huijsing and Schade do not teach a control signal generator; however, it would have been obvious that there is one since control signals need to be generated for the switches to work correctly.

For **claim 14**, Huijsing teaches the input stage (Huijsing, figure 1). Huijsing does not teach a switching means; however, in the same field of endeavor, Schade teaches an amplifier with switching means (Schade, figure 1) configured to operate in either a first mode or a second mode responsive to the switching signal (it is obvious that the switch has two stages, therefore, two modes), and the NMOS and PMOS transistor doublets are both kept active in each of the modes (Schade, figure 1), and wherein the plurality of switches are configured, in the first mode, to direct the analog input signals to the first

differential input and to connect a first reference voltage to the second different input, and the plurality of switches are configured, in the second mode, to direct the analog input signals to the second differential input and to connect a second reference voltage to the first differential input (Schade, figure 1).

For **claim 15,** Huijsing teaches the first differential input is formed by the gates of the NMOS transistor doublet and the second differential input is formed by the gates of the PMOS transistor doublet (Huijsing, figure 2).

3. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat# 4555673/ *or "Huijsing" hereinafter*) in view of Schade, JR. (US Pat# 4392112/ *or "Schade" hereinafter*) and Miyazawa et al. (US Pub# 20020196247 A1/ *or "Miyazawa" hereinafter*).

For **claim 4,** Schade teaches an amplifier with switching means for receiving and selectively directing analog input signals only to one of either said first differential input or to second differential input (Schade, figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention that the transistors are connectable to any of the plurality of switches. Huijsing and Schade does not teach the gates of the transistors being connected to the same node; however, in the same field of endeavor, Miyazawa teaches MOS transistor doublets wherein the gates of the first doublet are connected to a first node and the gates of the second doublet are connected to a second

node (Miyazawa, figure 1, items M5, M6, phi3, M2, M4, and phi2). Miyazawa teaches that these transistors can be either NMOS or PMOS (Miyazawa, page 4, paragraph [0049], lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huijsing and Schade with Miyazawa because the addition would allow for an increase in control as to which transistor pairs to use.

For **claim 13,** Miyazawa teaches that the circuit is part of a display panel module (Miyazawa, page 5, paragraph [0063], lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huijsing and Schade with Miyazawa because the addition would allow for an increase in control as to which transistor pairs to use.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat# 4555673/ *or "Huijsing" hereinafter*) in view of Schade, JR. (US Pat# 4392112/ *or "Schade" hereinafter*) and applicant admitted prior art (*AAPA hereinafter*).

For **claim 11,** Huijsing and Schade does not teach a gate driver bank or an LCD panel; however, in the same field of endeavor, AAPA teaches that it is prior art for a conventional LCD to comprise of a gate driver bank and an LCD panel (AAPA, figure 4). AAPA also teaches a standard rail-to-rail input stage circuit (which Huijsing teaches) used in LCD (AAPA, figure 3). Therefore, it would have been obvious to modify Huijsing to be included in a conventional LCD driver circuit. It would have been obvious

to one of ordinary skill in the art at the time of the invention to modify Huijsing and Schade with AAPA because all deal with the same subject matter and the addition of the AAPA would increase the effectiveness of the gate driver.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Huijsing et al. (US Pat# 4555673) discloses a differential amplifier with rail-to-rail input capability and controlled transconductance; Shah et al. (US Pub# 20020026552 A1) discloses system and method for switching signals over twisted-pair wires.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Morris whose telephone number is (571)270-7171. The examiner can normally be reached on Monday-Friday, 7am-3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629